We claim:

- 1 1. A method for forming a semiconductor device comprising the 2 steps:
- 3 providing a substrate including a support region and an array
- 4 region having an array device diffusion region;
- 5 depositing a dielectric layer on said substrate;
- forming a patterned hardmask on said dielectric layer, said
- 7 patterned hardmask having a first opening that overlays at least a
- 8 portion of said array device diffusion region;
- 9 partially etching said dielectric layer selective to said
- 10 hardmask through said first opening to form a first recess in said
- 11 dielectric layer;
- 12 forming a second mask having a second opening at least
- 13 partially overlapping a portion of said first recess; and
- 14 subsequently etching said dielectric layer selective to said
- 15 hardmask through said second opening and through said portion of
- 16 said first recess,
- so that said portion of said first recess is extended through
- 18 said dielectric layer to form a second recess so that a
- 19 corresponding portion of said array device diffusion region is
- 20 exposed.
 - 1 2. The method of claim 1, further comprising, after said step of
 - 2 subsequently etching:
 - 3 removing said second mask;
 - 4 forming a first conductive feature in said second recess; and
 - 5 forming a second conductive feature in said first recess.
 - 1 3. The method of claim 1 wherein said second mask further comprises
- 2 a block mask over said support region.

- 1 4. The method of claim 2 wherein said first conductive feature
- 2 comprises a contact structure and said second conductive feature
- 3 comprises an interconnect structure.
- 1 5. The method of claim 1 wherein said second opening defines a
- 2 contact via.
- 1 6. The method of claim 1 wherein said patterned hardmask defines an
- 2 interconnect feature, and said second mask comprises a line-type
- 3 opening that is oriented to intersect said interconnect feature at
- 4 an angle.
- 1 7. The method of claim 6 wherein said angle is approximately 90
- 2 degrees.
- 1 8. The method of claim 1 wherein said second mask is completely
- 2 open in said array region.
- 1 9. The method of claim 3 wherein said second mask is completely
- 2 open in said array region.
- 1 10. The method of claim 1 wherein said array region further
- 2 comprises a memory device corresponding to said array device
- 3 diffusion region.
- 1 11. The method of claim 10 wherein said memory device comprises a
- 2 gate stack including an encapsulating dielectric positioned
- 3 adjacent to said array device diffusion region, and wherein said
- 4 method further comprises filling said second recess with a
- 5 conductive material to form a borderless contact.
- 1 12. The method of claim 10 wherein said memory device further

- 2 comprises a vertical transistor.
- 1 13. The method of claim 1 wherein said support region includes
- 2 a support device diffusion region, wherein said patterned
- 3 hardmask includes a third opening that overlays at least a portion
- 4 of said support device diffusion region and
- 5 said step of partially etching further comprises
- 6 simultaneously etching through said third opening to form a third
- 7 recess, and
- 8 wherein said second mask further comprises a fourth opening at
- 9 least partially overlapping a portion of said third recess and
- 10 said step of subsequently etching further comprises
- 11 simultaneously etching through said fourth opening and through said
- 12 portion of said third recess
- 13 so that said portion of said third recess is extended through
- 14 said dielectric layer to form a fourth recess so that a
- 15 corresponding portion of said support device diffusion region is
- 16 exposed.
- 1 14. The method of claim 13, further comprising, after said step of
- 2 subsequently etching:
- 3 removing said second mask;
- 4 depositing a conductive material in said second recess and
- 5 said fourth recess to form contact structures; and
- 6 depositing a second conductive material in said first recess
- 7 and said third recess to form interconnect structures.
- 1 15. A semiconductor device comprising:
- 2 a substrate including device diffusion region;
- 3 a dielectric layer on said substrate;
- 4 a contact structure formed in said dielectric layer; and
- 5 an interconnect structure formed in said dielectric layer over

- 6 said contact structure,
- 7 so that said contact structure is in contact with said device
- 8 diffusion region and said interconnect structure and wherein said
- 9 contact structure and said interconnect structure are aligned with
- 10 each other.
 - 1 16. The semiconductor device of claim 15, wherein said contact
 - 2 structure comprises a first conductive material and said
 - 3 interconnect structure comprises a second conductive material.
 - 1 17. The semiconductor device of claim 16, wherein said first
 - 2 conductive material and said second conductive material consist
 - 3 essentially of the same conductive material.
 - 1 18. The semiconductor device of claim 15, wherein said substrate
- 2 further comprises an array region including a vertical memory
- 3 device comprising said device diffusion region.
- 1 19. The semiconductor device of claim 15, wherein said substrate
 - 2 further comprises a gate stack including an encapsulating material
 - 3 adjacent to said device diffusion region wherein said contact
 - 4 structure and said encapsulating material share a boundary.
 - 1 20. The semiconductor device of claim 15, wherein said substrate
 - 2 further comprises an array region and a support region,
 - 3 said array region including an array device diffusion region
 - 4 and an array interconnect structure and
 - 5 said support region including a support device diffusion
 - 6 region and a support interconnect structure, and
 - 7 further comprising an array contact structure in contact with
 - 8 said array device diffusion region and said array interconnect
 - 9 structure and

- 10 further comprising a support contact structure in contact with
- 11 said support device diffusion region and said support interconnect
- 12 structure,
- wherein said array contact structure is aligned with said
- 14 array interconnect structure and said support contact structure is
- 15 aligned with said support interconnect structure.